What is claimed is:

1. A method of operating an LCD display, the LCD display including pixels arranged in an array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of the rows to enable the pixels within the selected row, and column driver circuitry for driving voltages onto the columns of the LCD display for storage in the pixels of the selected row, the columns of the LCD display including at least a first column located relatively proximate to the row driver circuitry and at least a second column located relatively distant from the row driver circuitry, the row enable signal being subject to a propagation delay as it is conducted along the selected row as measured between the first column and the second column, the method comprising the steps of:

a. applying the row enable signal to a first selected row of the LCD display via the row driver circuitry at a first predetermined time;

b. enabling a first column driver for applying a first driving voltage onto the first column of the LCD display at a second predetermined time to transfer the first driving voltage onto a first pixel located at an intersection of the first column with the first selected row;

c. enabling a second column driver for applying a second driving voltage onto the second column of the LCD display at a third predetermined time to transfer the second driving voltage onto a second pixel located at an intersection of the second column with the first selected row; and

d. delaying the third predetermined time beyond the second predetermined time by a delay that is approximately equal to the propagation delay.

2. The method of claim 1 wherein each voltage driven onto a selected column of the LCD display is also subject to a column propagation delay as it is conducted along the selected column as measured between the column driver circuitry and a row relatively distant from the column driver circuitry, the method further comprising the steps of:

e. applying a driving voltage onto the selected column of the LCD display at a first predetermined time; and

f. enabling a row driver for applying the row enable signal to the row relatively distant from the column driver at a second predetermined time delayed beyond the first predetermined time

by a delay that is approximately equal to the column propagation delay.

3. A method of operating an LCD display, the LCD display including pixels arranged in an array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of the rows to enable the pixels within the selected row, and column driver circuitry for driving voltages onto the columns of the LCD display for storage in the pixels of the selected row, the rows of the LCD display including at least a first row located relatively proximate to the column driver circuitry and at least a second row located relatively distant from the column driver circuitry, each voltage driven onto each columns of the LCD display being subject to a column propagation delay as it is conducted along the column as measured between the column driver circuitry and the second row, the method comprising the steps of:

a. applying driving voltages onto the columns of the LCD display at a first predetermined time; and

b. enabling a row driver for applying the row enable signal to the second row at a second predetermined time delayed beyond the first predetermined time by a delay that is approximately equal to the column propagation delay.

4. A method of compensating for propagation delay of a display line signal in a display having display elements accessed by an array of row display lines and column display lines, the method comprising the steps of:

a. generating a display line timing signal;

b. generating a first plurality of delayed display line timing signals in response to the display line timing signal; and

c. activating one of at least one row display line and at least one column display line in response to each of the first plurality of delayed display line timing signals.

5. The method of claim 4, wherein the step of generating a first plurality of delayed display line timing signals comprises:

approximating a first propagation delay for the display line signal to propagate from its source to a pixel associated with a first column display line; and

generating one of the first plurality of delayed display line timing signals to include a delay substantially equal to the approximated first propagation delay for the display line signal.

6. The method of claim 4, further comprising the steps of:

generating a second plurality of delayed display line timing signals in response to one or more of the first plurality of display line timing signals; and

activating one of the at least one row display line and at least one column display line in response to each of the second plurality of delayed display line timing signals.

7. The method of claim 4, further comprising the steps of:

tracking which display line of a plurality of display lines is next to be activated;

selecting one of the first plurality of display line timing signals in response to the tracking of which display line is next to be activated; and

activating a display line in response to the one of the first display line timing signals.

8. The method of claim 4, wherein the display line timing signal comprises signal components to activate a plurality of display lines at varying times.

9. The method of claim 8, further comprising the step of generating a second plurality of delayed display line timing signals in response to a first component of the display line timing signal.

10. The method of claim 9, further comprising the steps of:

removing the first component of the display line timing signal; and

generating a second plurality of delayed display line timing signals from a second component of the display line timing signal.

11. The method of claim 9, further comprising activating at least one display line in response to each of the second plurality of delayed display line timing signals.

12. A display line driver circuit for a display including display elements arranged in an array of rows and columns, the display line driver circuitry generating display line timing signals, and comprising:

a. a first plurality of delay elements operatively coupled together such that a signal propagating through the first plurality of delay elements is increasingly delayed as it propagates through each successive delay element;

b. a plurality of signal taps, each coupled between a selected pair of delay elements; and

c. at least one display line associated with each signal tap.

13. The display line driver circuit of claim 12 wherein each of the first plurality of delay elements comprises at least one of a resistive and a capacitive element.

14. The display line driver circuit of claim 12 wherein the first plurality of delay elements comprises a delay locked loop circuit.

15. The display line driver circuit of claim 12 wherein the display driver circuit is a column driver circuit and the at least one display line comprises a plurality of column line groups each associated with a column driver circuit.

16. The display line driver circuit of claim 15 further comprising a pulse generator coupled to each signal tap.

17. The display line driver circuit of claim 16 wherein each pulse generator is coupled to its respective signal tap through an inverter.

18. The display line driver circuit of claim 14 further comprising a delay locked loop adjustment circuit.

19. The display line driver circuit of claim 18 wherein the delay locked loop circuit includes an input and an output, and wherein the delay locked loop adjustment circuit comprises:

a calibration pulse generator coupled between an input of the delay locked loop circuit and a switch, wherein the calibration pulse generator is configured to selectively activate the calibration circuit in response to an input to the delay locked loop circuit;

a first comparator coupled to an output of the delay locked loop circuit;

a variable impedance element coupled between an inverting input of a second comparator and a first reference voltage;

a first fixed impedance element coupled between a second reference voltage and a non-inverting input to the second comparator and

a second fixed impedance coupled between the non-inverting input to of the second comparator and the first reference voltage, wherein an output of the second comparator is coupled to an inverting input of the first comparator.

a. a calibration pulse generator coupled to the input of the delay locked loop circuit;

b. a first comparator having an inverting input, a non-inverting input, and an output, the non-inverting input being coupled to the output of the delay locked loop circuit;

c. a second comparator having an inverting input, a non-inverting input, and an output, the output of the second comparator being coupled to the inverting input of the first comparator;

d. a variable impedance element coupled between the inverting input of the second comparator and a first reference voltage;

e. a first impedance element coupled between a second reference voltage and the non-inverting input of the second comparator; and

f. a second fixed impedance coupled between the non-inverting input of the second comparator and the first reference voltage.

20. The display line driver circuit of claim 18 wherein the delay locked loop adjustment circuit comprises a variable resistor coupled in parallel with a capacitor.

21. The display line driver circuit of claim 20 wherein the delay locked loop adjustment circuit includes a variable resistance, the delay locked loop adjustment circuit being configured to increase a relative delay of the delay elements as the variable resistance is increased, and to decrease the relative delay of the delay elements as the variable resistance is decreased.

22. The display line driver circuit of claim 15, wherein each column line driver group circuit comprises:

a. a second plurality of successive delay elements operatively coupled together such that a signal propagating through the second plurality of delay elements is increasingly delayed as it propagates through each successive delay element;

b. a plurality of signal taps each coupled between a selected pair of successive delay elements within the second plurality of successive delay elements; and

c. at least one column signal line associated with each signal tap.

23. The display line driver circuit of claim 12 wherein the display line driver circuit is a row driver circuit, and wherein the at least one display line associated with each signal tap includes a plurality of row line groups, each of the plurality of row line groups being associated with a signal tap, and each of the plurality of row line groups having a plurality of row lines associated therewith.

24. The display driver of claim 23, wherein the row driver circuit sequentially initiates each row of each plurality of row lines with a signal having a delay corresponding to the row line group with which it is associated.

25. The display driver of claim 24, further comprising a row counter circuit for tracking the sequential initiation of row lines and for selecting an appropriate signal tap through which a row

initiation signal is to be received for each row line.

26. A display having pixels arranged in an array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of the rows to enable the pixels within the selected row, and column driver circuitry for driving voltages onto the columns of the display for storage in the pixels of the selected row, the columns of the display including at least a first column located relatively proximate to the row driver circuitry and at least a second column located relatively distant from the row driver circuitry, the row enable signal being subject to a propagation delay as it is conducted along the selected row as measured between the first column and the second column, the display comprising:

a. a first plurality of delay elements within the column driver circuitry which are operatively coupled together such that a signal propagating through the first plurality of delay elements is increasingly delayed as it propagates through each successive delay element; and

b. a signal tap associated with the second column coupled at a selected point between two of the delay elements such that the delay of the signal propagating through the first plurality of delay elements at that selected point is substantially equal to the propagation delay of the row enable signal when it reaches the second column.

27. The display of claim 26, wherein the first plurality of delay elements comprises at least one element selected from the group of elements that includes resistive and capacitive elements.

28. The display of claim 26, wherein the first plurality of delay elements comprises a delay locked loop circuit.

29. The display of claim 26 further comprising a group of columns associated with a column group driver circuit for driving voltages onto each column of the group, said group of columns including the second column.

30. The display of claim 29 further comprising a first pulse generator coupled to the signal tap.

31. The display of claim 30 further comprising a second pulse generator coupled to the signal tap through an inverter.

32. The display of claim 29 further comprising a delay locked loop adjustment circuit.

33. The display of claim 32 wherein the delay locked loop adjustment circuit comprises:

a. a calibration pulse generator coupled to the input of the delay locked loop circuit;

b. a first comparator having an inverting input, a non-inverting input, and an output, the non-inverting input being coupled to the output of the delay locked loop circuit;

c. a second comparator having an inverting input, a non-inverting input, and an output, the output of the second comparator being coupled to the inverting input of the first comparator;

d. a variable impedance element coupled between the inverting input of the second comparator and a first reference voltage;

e. a first impedance element coupled between a second reference voltage and the non-inverting input of the second comparator; and

f. a second fixed impedance coupled between the non-inverting input of the second comparator and the first reference voltage.

34. The display of claim 32 wherein the delay locked loop adjustment circuit comprises a variable resistor coupled in parallel with a fixed capacitor.

35. The display of claim 34 wherein the delay locked loop adjustment circuit includes a variable resistance, the delay locked loop adjustment circuit being configured to increase a relative delay of the delay elements as the resistance of the variable resistor is increased, and to decrease the relative delay of the delay elements as the resistance of the variable resistor is decreased.

36. The display of claim 29, wherein the column driver group circuit comprises:

a. a second plurality of successive delay elements operatively coupled together such that a signal propagating through the second plurality of delay elements is increasingly delayed as it propagates through each successive delay element;

b. a signal tap associated with a third column among the column group and coupled at a selected point between two of the successive delay elements within the second plurality of successive delay elements; such that the delay of the signal propagating through the second plurality of successive delay elements at that selected point is substantially equal to the propagation delay of the row enable signal when it reaches the third column.

37. The display of claim 26 wherein the row driver circuitry is configured to sequentially initiate each row associated with the row driver circuitry at predetermined intervals, the row driver circuitry having associated therewith at least a first row located relatively proximate to the column driver circuitry and at least a second row located relatively distant from the column driver circuitry, each voltage driven onto a column being subject to a propagation delay as it is conducted along the selected column as measured between the first row and the second row, the display further comprising:

a. a plurality of successive row signal delay elements within the row driver circuitry which are operatively coupled together such that a signal propagating through the plurality of successive row signal delay elements is increasingly delayed as it propagates through each successive row delay element;

b. a plurality of signal taps associated with selected points among the plurality of successive row signal delay elements; and

c. circuitry configured to select a first signal tap from among the plurality of signal taps which will approximate the propagation delay of the voltage driven onto a column as it reaches the second row.

38. A display signal timing controller for a display having a plurality of display elements

arranged in an array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of the rows in response to a row timing signal, the row enable signal being subject to a propagation delay as it is conducted along the row, and column driver circuitry for driving voltages onto the columns of the display for storage in the pixels of the selected row in response to a column timing signal, the voltage driven onto the column also being subject to a propagation delay as it is conducted along the column, the display signal timing controller comprising:

a. a plurality of delay elements coupled in series for delaying a first display timing signal;

b. a plurality of taps coupled between select delay elements of the plurality of delay elements for tapping delayed portions of the first display timing signal; and

c. output circuitry configured to generate a second display timing signal in response to the first display timing signal, the second display timing signal having signal components corresponding to each of the delayed portions of the tapped first display timing signal.

39. The display signal timing controller of claim 38 further comprising a plurality of display driver circuits, wherein each of the display driver circuits comprises:

a. input circuitry configured to generate a third display timing signal in response to a signal component of the second display timing signal;

b. a second plurality of delay elements for delaying the third display timing signal; and

c. a plurality of taps coupled between select delay elements of the second plurality of delay elements for tapping delayed portions of the third display timing signal.

40. A display having pixels arranged in an array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of the rows to enable the pixels within the selected row, and column driver circuitry for driving voltages onto the columns of the display for storage in the pixels of the selected row, the rows of the display including at least a first row located relatively proximate to the column driver circuitry and at least a second row located relatively distant from the column driver circuitry, each voltage driven onto a column being subject to a propagation delay as it is conducted along the column as measured between the first row and the second row, the display

comprising:

a. a plurality of successive row signal delay elements within the row driver circuitry which are operatively coupled together such that a signal propagating through the plurality of successive row signal delay elements is increasingly delayed as it propagates through each successive row signal delay element;

b. a plurality of signal taps associated with selected points among the plurality of successive row signal delay elements; and

c. circuitry configured to select a first signal tap from among the plurality of signal taps which will approximate the propagation delay of the voltage driven onto a column as it reaches the second row.